REMARKS

An excess claim fee payment letter is submitted herewith for seven (7) excess independent claims.

Claims 1-14 are presently pending in the application. Claims 1-7 have been amended to more particularly define the invention. Claims 8-14 have been added to assure Applicant the degree of protection to which his invention entitles him.

It is noted that the claim amendments are made only to assure grammatical and idiomatic English and improved form under United States practice, and are not made to distinguish the invention over the prior art or narrow the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

The Office Action discusses the requirements for an Abstract, but makes no specific objection to the present Abstract. However, a new Abstract is submitted herewith, including amendments to assure grammatical and idiomatic English.

Objection was made to the specification under 35 U.S.C. §112, first paragraph, with the contention the specification included terms which are not clear, concise, and exact. The specification has been amended to use clear, concise, and exact terms, as well as to assure grammatical and Idiomatic English and improved form under United States practice. Thus, this objection is overcome.

In view of the extent of the amendments to the specification, a Substitute Specification is submitted herewith, together with a marked copy of the original specification.

The undersigned attorney affirms that the Substitute Specification contains no new matter.

Objection was made to the claims due to typographical errors. These have been corrected in the amended claims.

Claims 1-7 were rejected under U.S.C. §112, second paragraph, with the contentions that it is unclear what the function of the plural logic gates is, that the logic gates could be another flip-flop or any type of functional logic block, and that the function or type was not clearly disclosed in the specification. These contentions, and the rejection based on them, are traversed.

The specification describes the operation of the logic gates at page 14, line 5 to page 15, line 19. Claims 1-7 have been amended to set out that the flip-flops are connected in series through the logic circuit.

It is accordingly submitted that this rejection should be withdrawn.

Claims 1-2 and 4 were rejected under 35 U.S.C. §102(e) as being anticipated by Whetsel, U.S. Patent No. 6,199,182. This rejection is respectfully traversed.

Whetsel discloses probless testing of pad buffers on wafers. Although Whetsel discloses an array of die on a wafer, for example in Figures 26-29, those die are connected by a scan path which connects the die in series in the manner of the acknowledged prior art of Figure 1 of the present application.

Thus, as seen in Figures 26 and 28 of Whetsel, each array consists of a plurality of rows, each row including a plurality of die. The scan path connects the first die of each row to the second die of that row, and that die is connected to the next die of the row, which is connected to the next die of the row, etc., continuing to the last die of the row which is

connected to the first die of the next row. The scan path continues in the same manner to the last row, the last die of which is connected to an output terminal. This scan path is the equivalent of the prior art of Figure 1 of the present application.

The scan path of the test circuit of the claimed invention differs in an unobvious manner from that of Whetsel and the acknowledged prior art. Thus, in one exemplary embodiment, the scan path connects the output terminal of the flip-flop located at an end of the first stage with the scan output terminal of said logical integrated circuit

In another exemplary embodiment, the scan path connects the scan input terminal of said logical integrated circuit with the input terminal of the flip-flop located at the head of the nth stage.

In yet another exemplary embodiment, the scan path connects the scan input with the input terminal of the flip-flop located at the head of the nth stage. From the output of the flip-flop located at the end of the nth stage, the scan path further connects the flip-flops in the second to the (n-1)th stages in series. The scan path then connects the output terminal of the flip-flop located at the end of the (n-1)th stage with the input terminal of the flip-flop located at the head of the first stage. The scan path finally connects the output terminal of the flip-flop located at the end of the first stage with the scan output terminal of said logical integrated circuit.

These exemplary embodiments provide scan paths that differ from that of Whetsel in an unobvious manner. The claimed scan paths permit faster testing, as set forth in the specification, for example at page 18, line 24 to page 19, line 7.

It is noted that there was no rejection of claims 3 and 5-7 on prior art. Since the

rejections under 35 U.S.C. §112 have been overcome, claims 3 and 5-7 are allowable.

In view of the foregoing, Applicant submits that claims 1-14, all the claims presently pending in the application, are patentably distinct over the prior art of record and are allowable, and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below to discuss any other changes deemed necessary for allowance in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. The Commissioner is authorized to charge any deficiency in fees, including extension of time fees, or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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